TUTORIAL 7

Theoretical Questions:

Q1. Explain on the basic operation of the n-channel JFET. Draw the drain characteristics of the mentioned JFET type and denote the important parameters on the graph.

Q2. Explain why the JFET is called a unipolar device. Your explanation must be based on the n-channel or p-channel device which is biased to operate as an amplifier.

Q3. What is one advantage of FET over BJT?

Q4. What is the main advantage of using self-biasing in a JFET amplifier circuit? Draw the self-biasing circuit.

Q5. State the three basic configurations of the JFET circuit. Compare and give brief description on the circuits' voltage gain, input and output impedances. State the main application for each configuration.

Q6. Describe in detail, with the help of appropriate illustrations, the operation of the n-channel E-MOSFET under the following biasing conditions:

(a) drain and source are grounded, no biasing voltage at the gate
(b) drain and source are grounded, small positive voltage at the gate
(c) small positive voltage at the gate, small positive voltage at the drain and source
(d) small positive voltage at the gate, V_{DS} increased from the value in (c)

Q7. Draw the schematic of the p-channel E-MOSFET in its typical operation. Explain on the drain and transfer characteristics of this circuit.

Q8. Draw the cross section and the drain characteristics of an n-channel E-MOSFET at the different biasing condition specified below:

(i) $V_{GS} < V_{GS(th)}$ and $V_{DS} > 0$

(ii) $V_{GS} > V_{GS(th)}$ and $V_{DS} > V_{DS(sat)}$

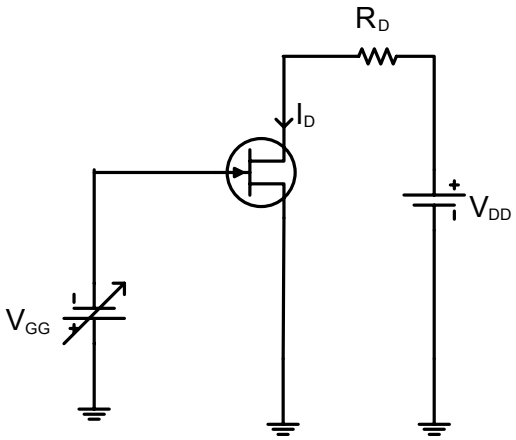
(iii) $V_{GS} > V_{GS(th)}$ and $V_{DS} = V_{DS(sat)}$

(iv) $V_{GS} > V_{GS(th)}$ and $V_{DS} > V_{DS(sat)}$

Q9. Draw the I_D versus V_{DS} curve for an ideal n-channel E-MOSFET (NMOS). Label the operating mode regions and write the I_D expression for each region.

Q10. With the help of illustrations, explain briefly on the operation of the DE and E MOSFETs as amplifiers and comment on the differences.

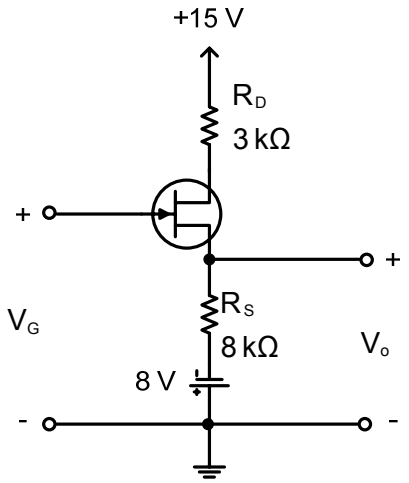
Q11. For the circuit shown below,
(a)give detailed explanation on the reason why I_D will decrease with the increment of V_{GG} at a fixed V_{DD}.
(b)what will happen if $V_{GG} = V_{GS(off)}$?



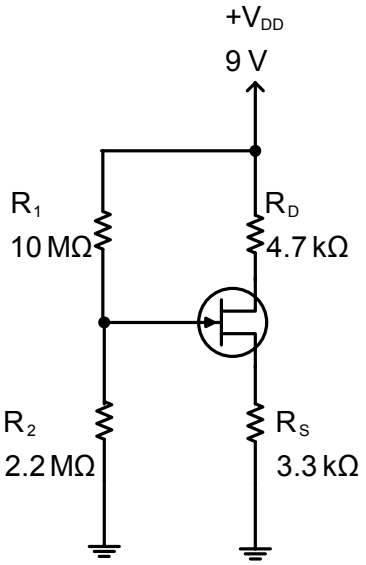
Q12. How is the drain current controlled in the n-channel JFET? Use illustrations to help you in giving your explanations.

Calculations:

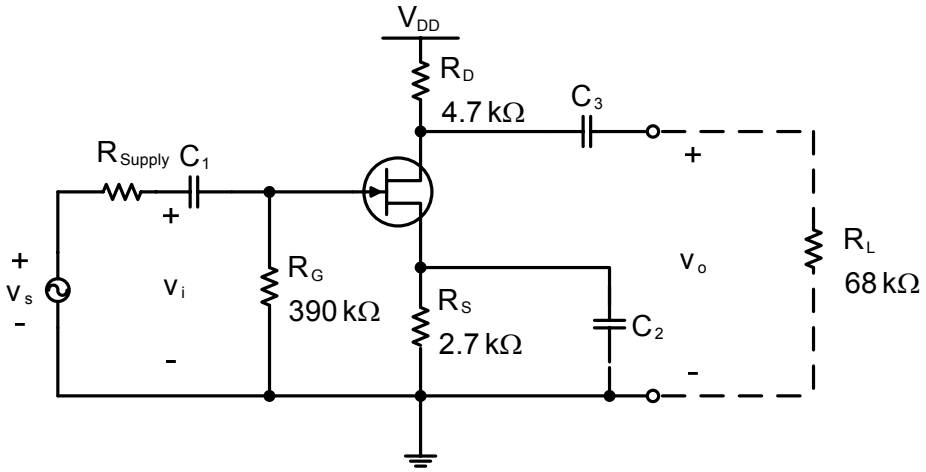
Q1. The JFET in the following diagram has the following characteristics, $I_{DSS} = 5mA$ and $V_{GS(off)} = -3V$. Determine V_{GSQ} and V_O if
(a) $V_G = 0\ V$
(b) $V_G = 10\ V$



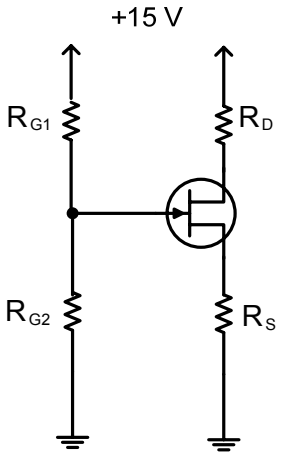
Q2. Given the drain to ground voltage is equivalent to 5 V for the circuit below. Calculate I_D, V_{GS}, V_{DS} and V_S for this circuit.



Q3. Calculate the voltage gain and the input and output impedances for the common source circuit shown below. $R_{GS} = 1000\ M\Omega$, $g_m = 4000\ \mu S$ and $r_{ds} = 80\ k\Omega$. Determine the voltage gain if C_2 is absent.

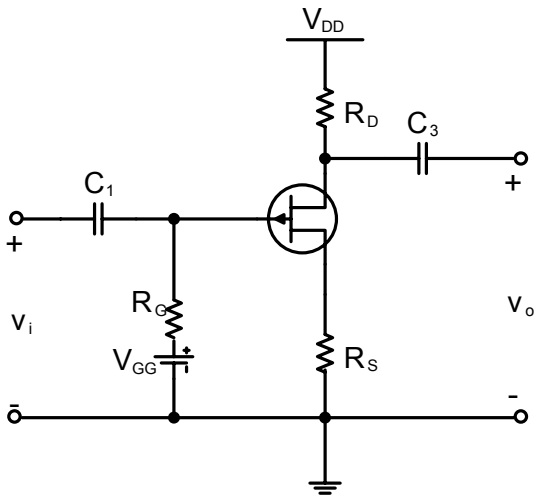


Q4. The JFET in the following diagram has V_p = -3 V and $I_{DSS} = 9\ mA$. Calculate the value of all the resistors so that $V_G = 5\ V, I_D = 4\ mA$ and $V_D = 11\ V$. The design has 0.05 mA flowing through the voltage divider.



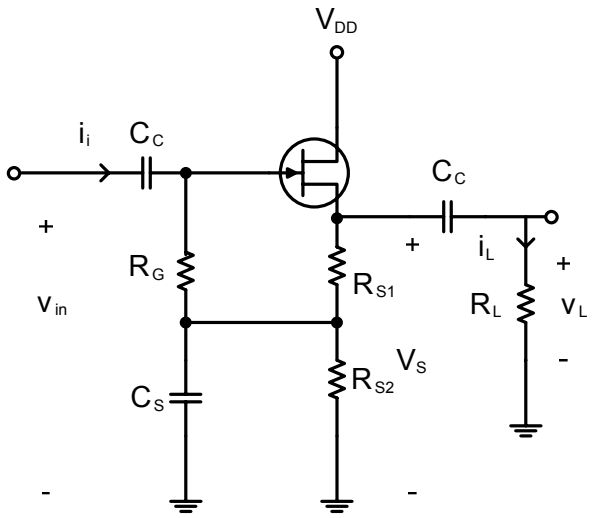
Q5. The gate current can be ignored for the JFET in the circuit below. If $V_{DD} = -20\ V, I_{DSS} = 10\ mA, I_{DQ} = 8\ mA, V_{GS(off)} = 4\ V, R_S = 0\ \Omega$ and $R_D = 1.5\ k\Omega$, determine

(i) V_{GG} and
(ii) V_{DSQ}



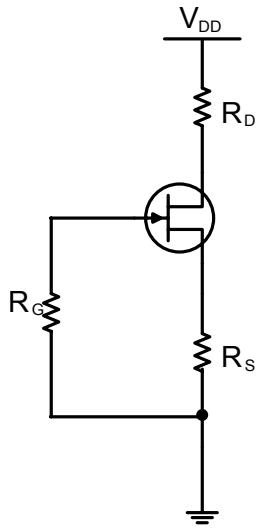
Q6. For the circuit shown below,
$R_G >> R_{S1}, R_{S2}, I_{DSS} = 10\ mA, V_{GS(off)} = -4\ V, V_{DD} = 15\ V, V_{DSQ} = 10\ V$ and $V_{GSQ} = -2\ V$.
Determine:

(a) V_S
(b) R_{S1}
(c) R_{S2}

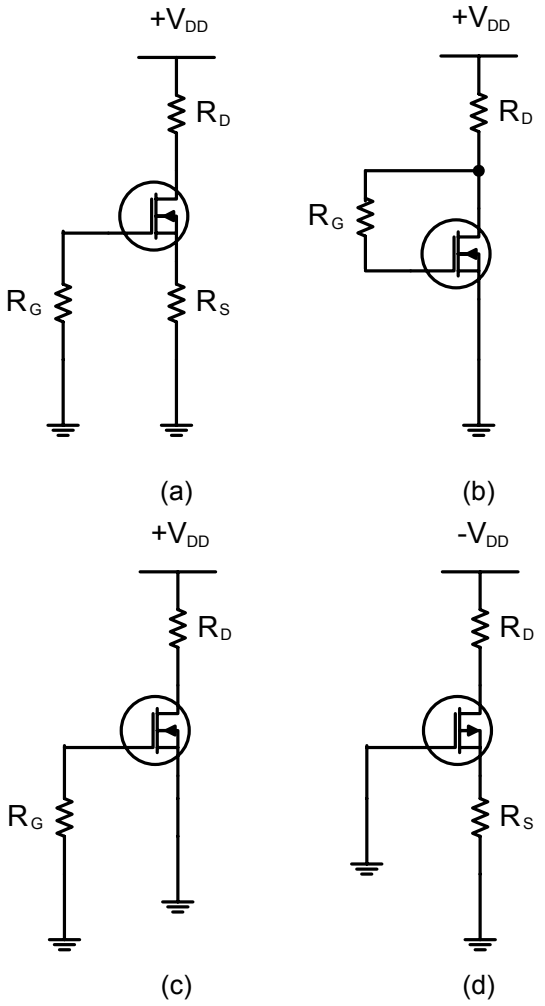


Q7. (a)Self-biasing is implemented on the following JFET circuit. Assume that the gate current can be neglected ($I_G = 0$). Show that if $V_{DD} > 0$, $V_{GS} < 0$. This condition will enable correct device biasing.

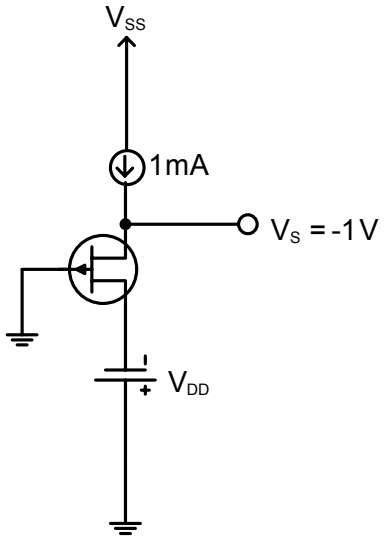
(b)If $R_D = 3\,\text{k}\Omega, R_S = 1\,\text{k}\Omega, V_{DD} = 15\text{ V}$ and $V_{DSQ} = 7\text{ V}$, calculate I_{DQ} and V_{GSQ}.



Q8. Referring to the following circuits, determine the DE MOSFET's mode of operation (depletion, enhancement or zero). Give explanation to your answer. Assume R_G is very large that the current flowing through it can be neglected resulting in $V_{RG} \approx 0$.

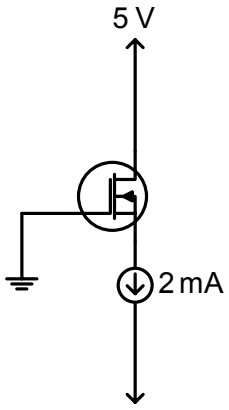


Q9. The JFET in the following circuit has V_p = -3 V. If V_S = -1 V when the device is in its pinched-off region, calculate I_{DSS}.



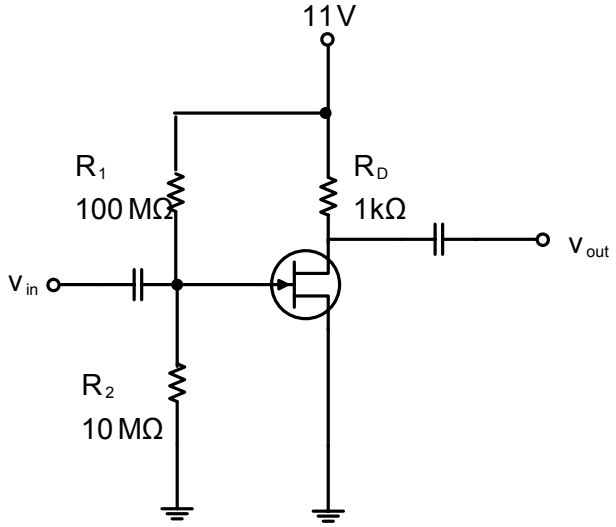
Q10. For a JFET that is operating at V_{GS} = -1 V, has V_p = -2 V and I_{DSS} = 8 mA, determine the variation required in the V_{GS} to increase the I_D by 0.4 mA. What is the variation required in the V_{GS} to reduce the I_D by 0.4 mA from the same initial value. Why is the variation in the V_{GS} different for both cases? What is the JFET type? Give explanations for your answers.

Q11. For the circuit shown below, $V_{GS(off)} = -2\,V$ and $K = 2\,mA/V^2$. Given $I_{DSS} = K\left[V_{GS(off)}\right]^2$. Neglecting the V_{DS} effect on I_D in the pinched-off region (also known as the constant current region or saturation region), calculate the voltage at the source of the transistor. Determine the operation mode of the device. Give two reasons for your answer.

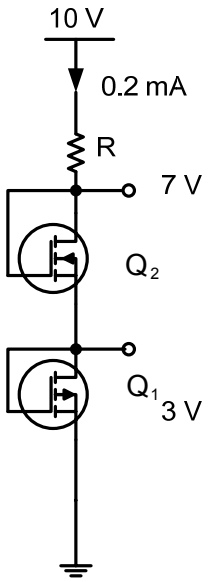


Q12. (a)Determine the voltages at the terminal, the transconductance and the voltage gain for the following DE-MOSFET circuit. Given: gain, $A_v = g_m \times R_D$, g_{m0} = 2000 μmho, $V_{GS(off)}$ = -4 V and I_{DSS} = 4 mA.

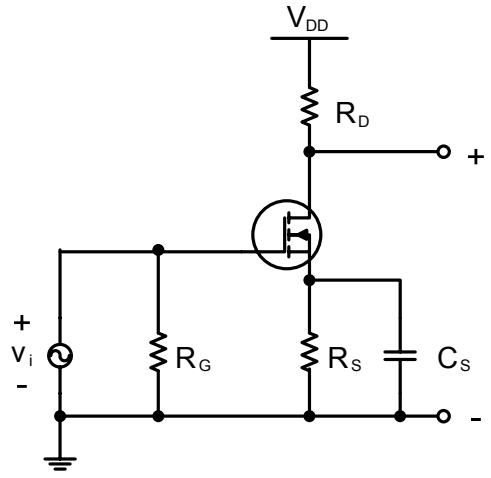
(b)Determine the transistor's mode of operation, i.e. whether it is in depletion or enhancement mode. Based on the results from the calculation in (a), give two reasons for your answer.



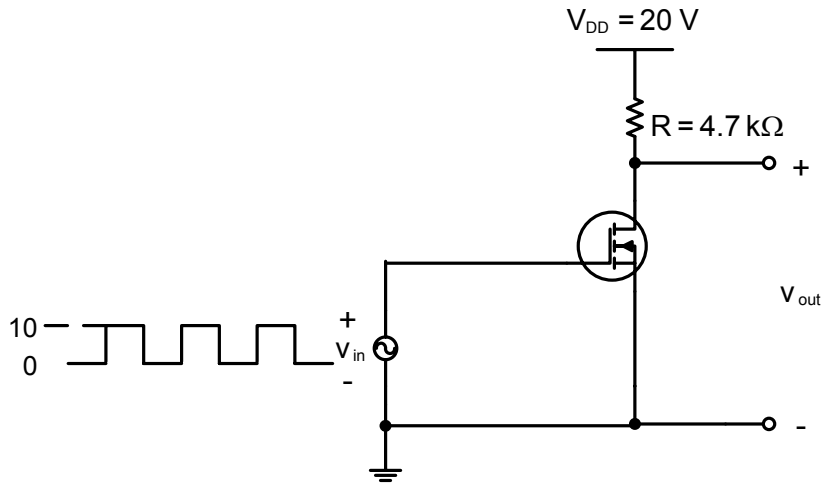
Q13. Each of the transistor in the circuit below has $V_{GS(th)} = 2\,V, \mu_n C_{ox} = 20\,\mu A/V^2, \lambda = 0$ and $L_1 = L_2 = 10\,\mu m$. Find the value of R and the required gate width for Q_1 and Q_2 to obtain the voltages and current as shown in the diagram.



Q14. In the common source amplifier of the circuit below, let $R_D = 3\,k\Omega, g_m = 2\times10^{-3}$ S and $r_{ds} = 30\,k\Omega$. Using the simplified, low-frequency small-signal equivalent circuit, find an expression for the voltage-gain ratio $A_v = v_o / v_{in}$ and then evaluate A_v.



Q15. E-MOSFETs are normally found operating as switches in digital ICs. Below is a typical switching circuit. Determine the waveform v_{out} for the shown v_{in}. Use the given drain characteristics to help you in your calculations. Repeat if R is changed to 10 kΩ.



Q16. Fixed biasing can be implemented on the E-MOSFET as shown in the diagram below. The drain characteristic of the E-MOSFET is included. $R_1 = 60\,k\Omega, R_2 = 40\,k\Omega, R_D = 3\,k\Omega, V_{DD} = 15\,V$. Assume $I_G = 0$.

(i) Calculate V_{GSQ}.

(ii) Determine V_{DSQ} and I_{DQ} from the drain characteristic.